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[File 35] Dissertation Abs Online 1861-2008/Feb

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[File 2] INSPEC 1898-2008/Nov W1

[File 6] NTIS 1964-2008/Nov W5

[File 144] Pascal 1973-2008/Nov W5

[File 34] SciSearch(R) Cited Ref Sci 1990-2008/Nov W4

[File 434] SciSearch(R) Cited Ref Sci 1974-1989/Dec

[File 256] TecInfoSource 82-2008/Jun

[File 95] TEME-Technology & Management 1989-2008/Nov W2

[File 99] Wilson Appl. Sci & Tech Abs 1983-2008/Oct

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Set Items Description
S1 144307 S (COMPRESS? OR ZIP? ? OR ZIPPED OR ZIPPING OR STUFF??? OR WINZIP? OR SQUEEZ? OR COMPACT???)(5N)(DATA OR DATUM OR FILE? ? OR INFORMATION OR CONTENT? ? OR RECORD? ? OR DATABASE? OR DATA()BASE? OR REPOSITOR? OR RESOURCE? ?)
S2 4462635 S (FILL????? OR MERGE?? OR MERGING OR POPULATE? OR COMPLET??? OR SUPPLY??? OR FURNISH???)
S3 12333 S S2(3N)(RANDOM?? OR PSEUDO()RANDOM?? OR PSEUDORANDOM?? OR ARBITRAR??? OR CHANCE OR DISCRETIONAR? OR AD()HOC OR UNSYSTEMATIC?)
S4 25076337 S (VECTOR? ? OR PATTERN? ? OR BIT? ? OR BYTE? ? OR SEQUENCE? ? OR SERIES OR STRING? ? OR DATA OR INFORMATION OR SIGNAL? ? OR CHARACTER? ? OR INPUT? ? OR SEGMENT? ? OR PROGRAM? ? OR VALUE? ?)
S5 17 S S2(5N)(CARE(2W)(BIT? ? OR BYTE? ? OR CODE? ?))
S6 14 S S5 AND S4
S7 0 S S3 AND S6
S8 404240 S S4 AND((LESS OR SMALLER OR LOWER OR LOOSEN OR BELOW OR FEWER OR MINOR?)(3N)(NUMBER? ? OR NUMERAL? ? OR CHARACTER? ? OR VALUE? ? OR DATA OR INFORMATION OR FIGURE? ? OR DIGIT? ? OR INTEGER? ? OR BIT? ? OR BYTE? ? OR WORD? ? OR CONTENT? ? OR AMOUNT? ? OR QUANTIT??? OR PATTERN? ? OR SEQUENCE? ? OR SERIES? ? OR STREAM? ?))

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Subject summary

? t s6/5,k/all
6/5,K/1 (Item 1 from file: 8) Links
Ei Compendex(R)

1209733791 E.I. COMPENDEX No: 20084711720529
Scheme of test data compression based on sharing-run-length code
Zhan, Wenfa; Liang, Huaguo; Shi, Feng; Huang, Zhengfeng; Ouyang, Yiming
Corresp. Author/Affil: Zhan, W.: School of Computer and Information, Hefei University of Technology, Hefei 230009, China
Corresp. Author email: zhanwenfa@gmail.com
Author email: hgliang@mail.hf.ah.cn; oyymbox@163.com
Jisuanji Yanjiu yu Fazhan/Computer Research and Development (Jisuanji Yanjiu yu Fazhan) (China) 2008 45/10 (1646-1653)
Publication Date: 20081001
Publisher: Science Press
CODEN: JYYFE ISSN: 1000-1239
Document Type: Article; Journal Record Type: Abstract
Language: Chinese Summary Language: Chinese; English
Number of References: 15
One of the major challenges in testing integrated circuits is dealing with the large test data size. To reduce the volume of test data, several test data compression schemes have been presented. But all of these schemes do not explore the relationship between consecutive runs. So a new scheme of test data compression/decompression, namely sharing-run-length code scheme (SRLCS) is presented, which is based on run length coding. It explores further the relationship between consecutive runs on the basis of traditional run length coding characteristic which uses shorter codeword to represent longer run length. Thus, only 1 bit needs to represent the whole later run in immediate two runs whose lengths are the same in this scheme. ATPG tools generate test patterns with many don't care bits, which are 95% to 99% of the bits in test data for large industrial circuits. So filling the don't care bits in test data appropriately can increase the probability of the consecutive runs whose lengths are the same. A strategy of filling don't care bits is also proposed for this scheme. Compared with other schemes, this scheme has some characteristics, such as high compression ratio and easy control and implementation. Theoretical analysis and experimental results for the Mintest test set of ISCAS-89 benchmark circuits show that the proposed scheme is a very efficient compression method.
Descriptors: Codes (symbols); Compression ratio (machinery); Digital signal processing; Electric network analysis; Integrated circuits; Motion estimation; Programming theory; Test facilities; Testing; *Data compression
Identifiers: Alternating run-length code; Frequency-directed run-length code; Golomb code; Run length coding; Sharing-run-length code; Test data compression
Classification Codes:
703.1.1 (Electric Network Analysis)
714.2 (Semiconductor Devices & Integrated Circuits)
716.1 (Information & Communication Theory)
721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))
722.3 (Data Communication, Equipment & Techniques)
722.4 (Digital Computers & Systems)
723.1 (Computer Programming)
723.2 (Data Processing)
402.1 (Industrial & Agricultural Buildings)
422.1 (Test Equipment)
422.2 (Test Methods)
423.1 (Test Equipment)
423.2 (Test Methods)
612.1 (Internal Combustion Engines, General)
618.1 (Compressors)
Scheme of test data compression based on sharing-run-length code
One of the major challenges in testing integrated circuits is dealing with the large test data size. To reduce the volume of test data, several test data compression schemes have been presented. But all of these schemes do not explore the relationship between consecutive runs. So a new scheme of test data compression/decompression, namely sharing-run-length code scheme (SRLCS) is presented, which is based on... ...length coding characteristic which uses shorter codeword to represent longer run length. Thus, only 1 bit needs to represent the whole later run in immediate two runs whose lengths are the same in this scheme. ATPG tools generate test patterns with many don't care bits, which are 95% to 99% of the bits in test data for large industrial circuits. So filling the don't care bits in test data appropriately can increase the probability of the consecutive runs whose lengths are the same. A strategy of filling don't care bits is also proposed for this scheme. Compared with other schemes, this scheme has some characteristics...
Descriptors: Codes (symbols); Compression ratio (machinery); Digital signal processing; Electric network analysis; Integrated circuits; Motion estimation; Programming theory; Test facilities; Testing; *Data compression
Identifiers: ...Frequency-directed run-length code; Golomb code; Run length coding; Sharing-run-length code; Test data compression

6/5,K/2 (Item 2 from file: 8) Links
Ei Compendex(R)

0018497485 E.I. COMPENDEX No: 20083111420958
Block marking and updating coding in test data compression for SoC
Issue Title: Proceedings of the 16th Asian Test Symposium, ATS 2007
Zhang, Lei; Liang, Huaguo; Zhan, Wenfa; Jiang, Cuiyun
Corresp. Author/Affil: Zhang, L.: School of Computer and Information, Hefei University of Technology, 230009 Hefei, China
Author email: hgliang@mail.hf.ah.cn; zhanwenfa@gmail.com
Conference Title: 16th Asian Test Symposium, ATS 2007
Conference Location: Beijing China Conference Date: 20071008-20071011
Sponsor: IEEE Comput. Soc. Test Technology Technical Council (TTTC); Institute of Computing Technology, Chinese Academy of Sciences
E.I. Conference No.: 72788
Proceedings of the Asian Test Symposium (Proc Asian Test Symp) (United States) 2007 , P2890 (467-470)
Publication Date: 20070101
Publisher: Inst. of Elec. and Elec. Eng. Computer Society
ISSN: 1081-7735 ISBN: 0769528902; 9780769528908
Item Identifier (DOI): 10.1109/ATS.2007.4388056
Article Number: 4388056
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Language: English Summary Language: English
Number of References: 10
A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show that the scheme is very effective. (c) 2007 IEEE.
Descriptors: Programming theory; Test facilities; Testing; Vectors; *Data compression
Identifiers: Benchmark circuits; Coding schemes; Test data; Test Data Compression; Test data in; Test sets
Classification Codes:
402.1 (Industrial & Agricultural Buildings)
422.2 (Test Methods)
716.1 (Information & Communication Theory)
721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))
921.1 (Algebra)
Block marking and updating coding in test data compression for SoC
A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show...
Descriptors: Programming theory; Test facilities; Testing; Vectors; *Data compression
Identifiers: Benchmark circuits; Coding schemes; Test data; Test Data Compression; Test data in; Test sets

6/5,K/3 (Item 3 from file: 8) Links
Ei Compendex(R)

0018368045 E.I. COMPENDEX No: 20082411306818
A selective scan slice encoding technique for test data volume and test power reduction
Badereddine, N.; Wang, Z.; Girard, P.; Chakrabarty, K.; Virazel, A.; Pravossoudovitch, S.; Landrault, C.
Corresp. Author/Affil: Virazel, A.: Laboratoire d'Informatique, de Robotique et de Microelectronique de Montpellier, Universite de Montpellier II/CNRS, 161, rue Ada, 34392 Montpellier Cedex 5, France
Corresp. Author email: virazel@lirmm.fr
Author email: Nabil.Badereddine@lirmm.fr; zw8@ee.duke.edu; Patrick.Girard@lirmm.fr; krish@ee.duke.edu; Serge.Pravossoudovitch@lirmm.fr; Christian.Landrault@lirmm.fr
Journal of Electronic Testing: Theory and Applications (JETTA) (J Electron Test Theory Appl JETTA) (Netherlands) 2008 24/4 (353-364)
Publication Date: 20080612
Publisher: Kluwer Academic Publishers
CODEN: JTTAE ISSN: 0923-8174 eISSN: 1573-0727
Item Identifier (DOI): 10.1007/s10836-007-5053-z
Document Type: Article; Journal Record Type: Abstract
Treatment: T; (Theoretical)
Language: English Summary Language: English
Number of References: 25

Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique (Wang Z, Chakrabarty K in Test data compression for IP embedded cores using selective encoding of scan slices. IEEE International Test Conference, paper 24.3, 2005) so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 14x reduction in test data volume and 98% test power reduction can be obtained simultaneously. (c) 2007 Springer Science+Business Media, LLC.
Descriptors: Data compression; Design for testability; Electric power utilization ; Electronic equipment manufacture; *Electronic equipment testing
Identifiers: Embedded Intellectual Property (IP) cores; Low power testing; Scan architectures; Test data compression
Classification Codes:
706.1 (Electric Power Systems)
714.2 (Semiconductor Devices & Integrated Circuits)
716.1 (Information & Communication Theory)
715 (Electronic Equipment, General Purpose & Industrial)
A selective scan slice encoding technique for test data volume and test power reduction
Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique (Wang Z, Chakrabarty K in Test data compression for IP embedded cores using selective encoding of scan slices. IEEE International Test Conference, paper 24.3, 2005) so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 14x reduction in test data volume and 98% test power reduction can be obtained simultaneously. (c) 2007 Springer Science+Business...
Descriptors: Data compression; Design for testability; Electric power utilization ; Electronic equipment manufacture; *Electronic equipment testing
Identifiers: Embedded Intellectual Property (IP) cores; Low power testing; Scan architectures; Test data compression

6/5,K/4 (Item 4 from file: 8) Links
Ei Compendex(R)

0018223239 E.I. COMPENDEX No: 20081011129582
California scan architecture for high quality and low power testing
Issue Title: 2007 IEEE International Test Conference, ITC
Cho, Kyoung Youn; Mitra, Subhasish; McCluskey, Edward J.
Corresp. Author/Affil: Cho, K.Y.: Center for Reliable Computing (CRC), Department of Electrical Engineering, Stanford University, Stanford, CA
Corresp. Author email: kycho@crc.stanford.edu
Author email: smitra@crc.stanford.edu; ejm@crc.stanford.edu
Conference Title: 2007 IEEE International Test Conference, ITC
Conference Location: Santa Clara, CA United States Conference Date: 20071023-20071025
Sponsor: IEEE Computer Society Test Technology Technical Council; IEEE Philadelphia Section
E.I. Conference No.: 71451
Proceedings - International Test Conference (Proc. Int. Test Conf.) (United States) 2008 , IEEE 07CH37892C , 25.3
Publication Date: 20080305
Publisher: Institute of Electrical and Electronics Engineers Inc.
CODEN: PITCF ISSN: 1089-3539 ISBN: 1424411289; 9781424411283
Item Identifier (DOI): 10.1109/TEST.2007.4437634
Article Number: 4437634
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Treatment: G; (General review)
Language: English Summary Language: English
Number of References: 29
This paper presents a scan architecture-California scan - that achieves high quality and low power testing by modifying test patterns in the test application process. The architecture is feasible because most of the bits in the test patterns generated by ATPG tools are don't-care bits. Scan shift-in patterns have their don 't- care bits assigned using the repeat-fill technique, reducing switching activity during the scan shift-in operation; the scan shift-in patterns are altered to toggle-fill patterns when they are applied to the combinational logic, improving defect coverage. (c) 2007 IEEE.
Descriptors: Power control; Power generation; Power quality; Switching; *Design for testability
Identifiers: California scan architecture; Low power testing
Classification Codes:
706.1.2 (Electric Power Distribution)
714.2 (Semiconductor Devices & Integrated Circuits)
721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory))
731.3 (Specific Variables Control)

...scan architecture-California scan - that achieves high quality and low power testing by modifying test patterns in the test application process. The architecture is feasible because most of the bits in the test patterns generated by ATPG tools are don't-care bits . Scan shift-in patterns have their don 't-care bits assigned using the repeat-fill technique, reducing switching activity during the scan shift-in operation; the scan shift-in patterns are altered to toggle-fill patterns when they are applied to the combinational logic, improving defect coverage. (c) 2007 IEEE.
Descriptors:

6/5,K/5 (Item 5 from file: 8) Links
Ei Compendex(R)

0017919407 E.I. COMPENDEX No: 20073610796886
Modeling power supply noise in delay testing
Wang, Jing; Walker, Duncan M.; Lu, Xiang; Majhi, Ananta; Kruseman, Bram; Gronthoud, Guido; Villagra, Luis Elvira; van de Wiel, Paul J.A.M.; Eichenberger, Stefan
Corresp. Author/Affil: Wang, J.: Dept. of Computer Science, Texas AandM University, College Station, TX 77843-3112, United States
Corresp. Author email: j0w2111@cs.tamu.edu
IEEE Design and Test of Computers (IEEE Des Test Comput) (United States) 2007 24/3 (226-234)
Publication Date: 20070910
Publisher: Inst. of Elec. and Elec. Eng. Computer Society
CODEN: IDTCE ISSN: 0740-7475
Item Identifier (DOI): 10.1109/MDT.2007.76
Document Type: Article; Journal Record Type: Abstract
Treatment: T; (Theoretical)
Language: English Summary Language: English
Number of References: 12
Excessive power supply noise can affect path delay in ICs. Silicon results show that filling of don't-care bits in test patterns can cause as much as 15% delay variation. Such extra delay may cause overkill during delay test. This article describes two types of low-cost noise models, compares them in model accuracy and application, and provides directions for model improvement. Excessive noise may come from compaction or filling during delay test generation. Experiments show how noise varies with different filling approaches, and how compaction is affected when the noise level for compacted tests is constrained. (c) 2007 IEEE.
Descriptors: Delay circuits; Microprocessor chips; Power supply circuits; Semiconducting silicon; Spurious signal noise; *Integrated circuit testing
Identifiers: Delay testing; Noise level; Power supply noise
Classification Codes:
712.1.1 (Single Element Semiconducting Materials)
713.5 (Other Electronic Circuits)
714.2 (Semiconductor Devices & Integrated Circuits)
721.3 (Computer Circuits)
Excessive power supply noise can affect path delay in ICs. Silicon results show that filling of don't-care bits in test patterns can cause as much as 15% delay variation. Such extra delay may cause overkill during...
Descriptors: Delay circuits; Microprocessor chips; Power supply circuits; Semiconducting silicon; Spurious signal noise; *Integrated circuit testing

6/5,K/6 (Item 6 from file: 8) Links
Ei Compendex(R)

0017670503 E.I. COMPENDEX No: 20071410524886
Power-aware test data compression for embedded IP cores
Issue Title: Proceedings of the 15th Asian Test Symposium 2006
Badereddine, N.; Wang, Z.; Girard, P.; Chakrabarty, K.; Virazel, A.; Pravossoudovitch, S.; Landrault, C.
Corresp. Author/Affil: Badereddine, N.: Laboratoire d'Informatique, de Robotique et de Microelectronique de Montpellier, Universite de Montpellier II, CNRS, 161, rue Ada, 34392 Montpellier Cedex 5, France
Corresp. Author email: n.badereddine@lirmm.fr
Author email: zw8@ee.duke.edu; p.girard@lirmm.fr; krish@ee.duke.edu; a.virazel@lirmm.fr; s.pravossoudovitch@lirmm.fr; c.landrault@lirmm.fr
Conference Title: 15th Asian Test Symposium 2006
Conference Location: Fukuoka Japan Conference Date: 20061120-20061123
E.I. Conference No.: 69203
Proceedings of the Asian Test Symposium (Proc Asian Test Symp) (United States) 2006 , IEEE P2628 2006/- (5-10)
Publication Date: 20061201
Publisher: Inst. of Elec. and Elec. Eng. Computer Society
ISSN: 1081-7735 ISBN: 0769526284; 9780769526287
Item Identifier (DOI): 10.1109/ATS.2006.260985
Article Number: 4030733
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Treatment: T; (Theoretical)
Language: English Summary Language: English
Number of References: 18

Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique [1] so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 20x reduction in test data volume and 95% test power reduction can be obtained simultaneously. (c) 2006 IEEE.
Descriptors: Data compression; Database systems; Electric power utilization; Embedded systems; Intellectual property; Optimization; *Internet protocols
Identifiers: Data volume; Intellectual Property (IP) cores; Power reduction
Classification Codes:
921.5 (Optimization Techniques)
902.3 (Legal Aspects)
723.3 (Database Systems)
722.3 (Data Communication, Equipment & Techniques)
716.1 (Information & Communication Theory)
706.1 (Electric Power Systems)
723 (Computer Software, Data Handling & Applications)
Power-aware test data compression for embedded IP cores
Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique [1] so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 20x reduction in test data volume and 95% test power reduction can be obtained simultaneously. (c) 2006 IEEE.
Descriptors: Data compression; Database systems; Electric power utilization; Embedded systems; Intellectual property; Optimization; *Internet protocols
Identifiers: Data volume; Intellectual Property (IP) cores; Power reduction

6/5,K/7 (Item 7 from file: 8) Links
Ei Compendex(R)

0015693533 E.I. COMPENDEX No: 2003457716359
ATPG padding and ATE vector repeat per port for reducing test data volume
Vranken, Harald; Hapke, Friedrich; Rogge, Soenke; Chindamo, Domenico; Volkerink, Erik
Corresp. Author/Affil: Vranken, H.: Philips Research, Digital Design and Test, Prof. Holstlaan 4, Way-41, 5656 AA Eindhoven, Netherlands
Corresp. Author email: harald.vranken@philips.com
Author email: friedrich.hapke@philips.com; soenke.rogge@philips.com; domenico chindamo@agilent.com; erik volkerink@agilent.com
Conference Title: Proceedings International Test Conference 2003
Conference Location: Charlotte, NC United States Conference Date: 20030930-20031002
Sponsor: IEEE Computer Society Test Technology Technical Council; IEEE Philadelphia Section
E.I. Conference No.: 61696
IEEE International Test Conference (TC) (IEEE Int Test Conf TC) (United States) 2003 , IEEE 03CH37494 (1069-1078)
Publication Date: 20031111
Publisher: Institute of Electrical and Electronics Engineers Inc.
CODEN: PITCF ISSN: 1089-3539
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Treatment: T; (Theoretical)
Language: English Summary Language: English
Number of References: 29
This paper presents an approach for reducing the test data volume that has to be stored in ATE vector memory for IC manufacturing testing. We exploit the capabilities of present ATE to assign groups of input pins to ports and to perform vector repeat per port. This allows run-length encoding of test stimuli per port. We improve the encoding by filling the don't-care bits in the test stimuli, such that longer run-lengths are obtained. We provide a probabilistic analysis of the performance of vector repeat per port with various ATPG padding types. We further discuss the impact of ATE architectures. The paper provides experimental data for a set of large industrial circuits, which shows an average reduction of the test stimulus data volume by a factor of 13.
Descriptors: Automatic testing; Transistors; Vectors; *Integrated circuits
Identifiers: Industrial circuits
Classification Codes:
714.2 (Semiconductor Devices & Integrated Circuits)
921.1 (Algebra)
422 (Strength of Building Materials; Test Equipment & Methods)

ATPG padding and ATE vector repeat per port for reducing test data volume
This paper presents an approach for reducing the test data volume that has to be stored in ATE vector memory for IC manufacturing testing. We exploit the capabilities of present ATE to assign groups of input pins to ports and to perform vector repeat per port. This allows run-length encoding of test stimuli per port. We improve the encoding by filling the don't-care bits in the test stimuli, such that longer run-lengths are obtained. We provide a probabilistic analysis of the performance of vector repeat per port with various ATPG padding types. We further discuss the impact of ATE architectures. The paper provides experimental data for a set of large industrial circuits, which shows an average reduction of the test stimulus data volume by a factor of 13.
Descriptors: Automatic testing; Transistors; Vectors; *Integrated circuits

6/5,K/8 (Item 1 from file: 2) Links
INSPEC

11062138
Title: California scan architecture for high quality and low power testing
Author Kyoung Youn Cho; Mitra, S.; McCluskey, E.J.
Author Affiliation: Dept. of Electr. Eng., Stanford Univ., Stanford, CA, USA
Conference Title: Proceedings International Test Conference 2007 p. 10 pp.
Publisher: IEEE , Piscataway, NJ, USA
Publication Date: 2007 Country of Publication: USA
ISBN: 978-1-4244-1127-6 Material Identity Number: YXA8-1900-223
Conference Title: International Test Conference 2007
Conference Date: 23-25 Oct. 2007 Conference Location: Santa Clara, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper presents a scan architecture - California scan - that achieves high quality and low power testing by modifying test patterns in the test application process. The architecture is feasible because most of the bits in the test patterns generated by ATPG tools are don't-care bits. Scan shift-in patterns have their don't- care bits assigned using the repeat-fill technique, reducing switching activity during the scan shift-in operation; the scan shift-in patterns are altered to toggle-fill patterns when they are applied to the combinational logic, improving defect coverage. (29 Refs)
Subfile: B C
Descriptors: automatic test pattern generation; combinational circuits; integrated circuit testing; logic design; low-power electronics
Identifiers: California scan architecture; high quality testing; low power testing; test application process; ATPG tool; scan shift-in pattern; repeat-fill technique; combinational logic
Class Codes: B1265A (Digital circuit design, modelling and testing); B1265B (Logic circuits); B7210A (Automatic test systems); C5210 (Logic design methods); C5120 (Logic and switching circuits); C7410H (Computerised instrumentation)

Abstract: ...scan architecture - California scan - that achieves high quality and low power testing by modifying test patterns in the test application process. The architecture is feasible because most of the bits in the test patterns generated by ATPG tools are don't-care bits . Scan shift-in patterns have their don't-care bits assigned using the repeat-fill technique, reducing switching activity during the scan shift-in operation; the scan shift-in patterns are altered to toggle-fill patterns when they are applied to the combinational logic, improving defect coverage.
Descriptors: automatic test pattern generation...
Identifiers: ...scan shift-in pattern;

6/5,K/9 (Item 2 from file: 2) Links
INSPEC

10876274
Title: Block marking and updating coding in test data compression for SoC
Author Lei Zhang; Huaguo Liang; Wenfa Zhan; Cuiyun Jiang
Author Affiliation: Hefei Univ. of Technol., Hefei, China
Conference Title: 2007 16th Asian Test Symposium p. 467-70
Publisher: IEEE , Piscataway, NJ, USA
Publication Date: 2007 Country of Publication: USA
ISBN: 978-0-7695-2890-8 Material Identity Number: YXA8-1900-562
Conference Title: 2007 16th Asian Test Symposium
Conference Date: 9-11 Oct. 2007 Conference Location: Beijing, China
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don 't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show that the scheme is very effective. (10 Refs)
Subfile: B C
Descriptors: automatic testing; data compression; decoding; integrated circuit testing; system-on-chip
Identifiers: block marking; updating coding; test data compression; SoC; decompression structure; ISCAS-89 benchmark

circuits
Class Codes: B7210A (Automatic test systems); B6120B (Codes); B1265A (Digital circuit design, modelling and testing); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); C7410H (Computerised instrumentation); C6130 (Data handling techniques)

Title: Block marking and updating coding in test data compression for SoC
Abstract: A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don 't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show...
Descriptors: ...data compression
Identifiers: ...test data compression...

6/5,K/10 (Item 3 from file: 2) Links
INSPEC

10308610
Title: Power-aware test data compression for embedded IP cores
Author Badereddine, N.; Wang, Z.; Girard, P.; Chakrabarty, K.; Virazel, A.; Pravossoudovitch, S.; Landrault, C.
Author Affiliation: Lab. d' Informatique, Univ. de Montpellier II, France
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Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, the authors propose in this paper to modify an existing test data compression technique so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded intellectual property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 20* reduction in test data volume and 95% test power reduction can be obtained simultaneously. (18 Refs)
Subfile: B C
Descriptors: benchmark testing; boundary scan testing; data compression; industrial property; logic testing; system-on-chip
Identifiers: scan architectures; test data compression; test data volume; power consumption reduction; scan testing; embedded intellectual property cores; benchmark circuits; industrial circuits
Class Codes: B1265A (Digital circuit design, modelling and testing); B1265F (Microprocessors and microcomputers); C5210 (Logic design methods); C5130 (Microprocessor chips)

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Descriptors: ...data compression
Identifiers: ...test data compression... ...test data volume...

6/5,K/11 (Item 4 from file: 2) Links
INSPEC

09014286 INSPEC Abstract Number: B2004-08-1265A-042
Title: ATPG padding and ATE vector repeat per port for reducing test data volume
Author Vranken, H.; Hapke, F.; Rogge, S.; Chindamo, D.; Volkerink, E.
Author Affiliation: Digital Design & Test, Philips Res., Eindhoven, Netherlands
Conference Title: Proceedings. International Test Conference 2003 (IEEE Cat. No.03CH37494) Part Vol.1 p. 1069-78 Vol.1
Publisher: IEEE , Piscataway, NJ, USA
Publication Date: 2003 Country of Publication: USA 2 vol. 1549 pp.

ISBN: 0 7803 8106 8 Material Identity Number: XX-2003-01341
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Conference Title: Proceedings. International Test Conference 2003
Conference Date: 30 Sept.-2 Oct. 2003 Conference Location: Charlotte, NC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T); Experimental (X)
Abstract: This paper presents an approach for reducing the test data volume that has to be stored in ATE vector memory for IC manufacturing testing. We exploit the capabilities of present ATE to assign groups of input pins to ports and to perform vector repeat per port. This allows run-length encoding of test stimuli per port. We improve the encoding by filling the don't-care bits in the test stimuli, such that longer run-lengths are obtained. We provide a probabilistic analysis of the performance of vector repeat per port with various ATPG padding types. We further discuss the impact of ATE architectures. The paper provides experimental data for a set of large industrial circuits, which shows an average reduction of the test stimulus data volume by a factor of 13. (29 Refs)
Subfile: B
Descriptors: automatic test equipment; automatic test pattern generation; integrated circuit testing; runlength codes; statistical analysis
Identifiers: ATPG padding; automatic test pattern generation; ATE vector; automatic test equipment; test data volume; IC manufacturing testing ; input pins; input ports; vector repeat per port; run-length encoding; test stimuli; longer run-lengths; probabilistic analysis; industrial circuits; test stimulus data volume
Class Codes: B1265A (Digital circuit design, modelling and testing); B7210A (Automatic test systems); B6120B (Codes); B0240 (Probability and statistics)

Title: ATPG padding and ATE vector repeat per port for reducing test data volume
Abstract: This paper presents an approach for reducing the test data volume that has to be stored in ATE vector memory for IC manufacturing testing. We exploit the capabilities of present ATE to assign groups of input pins to ports and to perform vector repeat per port. This allows run-length encoding of test stimuli per port. We improve the encoding by filling the don't-care bits in the test stimuli, such that longer run-lengths are obtained. We provide a probabilistic analysis of the performance of vector repeat per port with various ATPG padding types. We further discuss the impact of ATE architectures. The paper provides experimental data for a set of large industrial circuits, which shows an average reduction of the test stimulus data volume by a factor of 13.
Descriptors: ...automatic test pattern generation...
Identifiers: ...automatic test pattern generation... ...ATE vector; ... ...test data volume... ...input pins... ...input ports... ...vector repeat per port... ...test stimulus data volume

6/5,K/12 (Item 1 from file: 34) Links
Fulltext available through: STIC Full Text Retrieval Options
SciSearch(R) Cited Ref Sci

17887961 Genuine Article#: 307TJ Number of References: 25
A selective scan slice encoding technique for test data volume and test power reduction
Author: Badereddine N; Wang Z; Girard P; Chakrabarty K; Virazel A (REPRINT) ; Pravossoudovitch S; Landrault C
Corporate Source: Univ Montpellier 2,CNRS, Lab Informat Robot & Microelectron Montpellier,161 Rue Ada/F-34392 Montpellier 5//France/ (REPRINT); Univ Montpellier 2,CNRS, Lab Informat Robot & Microelectron Montpellier,F-34392 Montpellier 5//France/; Duke Univ,Dept Elect & Comp Engn,Durham//NC/27708
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ISSN: 0923-8174 Publication date: 20080800
Publisher: SPRINGER , VAN GODEWIJCKSTRAAT 30, 3311 GZ DORDRECHT, NETHERLANDS
Language: English Document Type: ARTICLE
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Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique (Wang Z, Chakrabarty K in Test data compression for IP embedded cores using selective encoding of scan slices. IEEE International Test Conference, paper 24.3, 2005) so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 14x reduction in test data volume and 98% test power reduction can be obtained simultaneously.
Descriptors--Author Keywords: DfT ; scan ; low power testing ; test data compression
Identifiers-- KeyWord Plus(R): ARCHITECTURE; COMPRESSION
Cited References:
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A selective scan slice encoding technique for test data volume and test power reduction
Abstract: Scan architectures, though widely used in modern designs for testing purpose, are expensive in test data volume and power consumption. To solve these problems, we propose in this paper to modify an existing test data compression technique (Wang Z, Chakrabarty K in Test data compression for IP embedded cores using selective encoding of scan slices. IEEE International Test Conference, paper 24.3, 2005) so that it can simultaneously address test data volume and power consumption reduction for scan testing of embedded Intellectual Property (IP) cores. Compared to the initial solution that fill don't-care bits with the aim of reducing only test data volume, here the assignment is performed to minimize also the power consumption. The proposed power-aware test data compression technique is applied to the ISCAS'89 and ITC'99 benchmark circuits and on a number of industrial circuits. Results show that up to 14x reduction in test data volume and 98% test power reduction can be obtained simultaneously.
Identifiers--

6/5,K/13 (Item 1 from file: 95) Links
TEME-Technology & Management

02320661 20080410104
Block marking and updating coding in test data compression for SoC
Zhang, Lei; Liang, Huaguo; Zhan, Wenfa; Jiang, Cuiyun
Hefei University of Technology, CN
16th Asian Test Symposium 2007, Beijing, CN, 9-11 Oct, 2007 , 2007
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 978-0-7695-2890-8
Abstract:
A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don 't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show that the scheme is very effective.
Descriptors: ATS--AUTOMATIC TEST SYSTEM; DATA COMPRESSION; DECODING--COMPUTING; INTEGRATED CIRCUIT TESTING
Identifiers: SYSTEM AUF EINEM CHIP; VERSUCHSDATEN; Automatische Pruefung; Datenreduktion
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Abstract:
A novel test data compression coding scheme, block marking and updating coding, is proposed in this paper. Test data in the test set was divided into successive fixed-length vectors, called blocks, and then they were marked according to their compatibility compared with a reference vector. An operation that is similar to difference and a technique that strategically fills in don 't-care bits are combined to increase the probabilities of compatibility or inverse compatibility. It effectively compresses test data and its decompression structure is very simple. Experimental results of ISCAS-89 benchmark circuits show...
Descriptors: ...AUTOMATIC TEST SYSTEM; DATA COMPRESSION; DECODING...
Identifiers:

6/5,K/14 (Item 2 from file: 95) Links
Fulltext available through: STIC Full Text Retrieval Options
TEME-Technology & Management

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Preventing Legionellosis
(Schutz vor Legionellen)
Stout, Janet E
University of Pittsburgh, PA, US

ASHRAE Journal, v49, n10, pp58-62 , 2007
Document type: journal article Language: English
Record type: Abstract
ISSN: 0001-2491
Abstract:
In order to better manage legionellosis, the ASHRAE Guideline 12-2000 is being converted to ASHRAE Standards Project Committee 188P, Minimizing the Risk of Legionellosis Associated with Building Water Systems. The current trend today is an evidence-based approach to legionella guidelines, wherein it requires, among other things, recommendations to be prospectively validated through controlled studies and be assessed objectively. Such an approach would also improve the utility of ASHRAE Guideline 12-2000 and make sure the strength or weakness of a recommendation with respect to scientific foundation. An evidence-based assessment can be best sited in the New York State Department of Health guidelines for the protection of patients from hospital-acquired Legionnaires' disease. It has recommended, among others for infection control, a quarterly culturing of the potable water system of transplant units for legionella species. For engineering environmental care and maintenance, it has recommended to store hot water at 60 degree C, among others. Each disinfectant method must undergo evaluation, including demonstrated efficacy in vitro, anecdotal experience in individual hospitals, controlled studies of sufficient duration in single hospitals and confirmatory reports from multiple hospitals. Although hard to implement initially, the benefits of an evidence-based standard include a sustained value based on scientific document and avoid the loss of credibility that will come when nonevidence-based recommendations fail.
Descriptors: DRINKABLE WATER; PROPHYLACTIC HEALTH CARE; BACILLUS; HYGIENE--SANITATION; DISINFECTION; STANDARDISATION--GENERAL; WATER SUPPLY; HEALTH CARE; CODE OF PRACTICE; PATIENTS; INFECTION; TRANSPLANTATION --SURGICAL; INSPECTION SPECIFICATIONS; TEST METHOD; HOSPITAL--PUBLIC BUILDING
Identifiers: ASHRAE STANDARD; THERMISCHE DESINFEKTION; Legionellenprophylaxe; ASHRAE Standard; Krankenhaus; Wasser-Desinfektion
Abstract:
...Although hard to implement initially, the benefits of an evidence-based standard include a sustained value based on scientific document and avoid the loss of credibility that will come when nonevidence...
Descriptors: ...GENERAL; WATER SUPPLY; HEALTH CARE; CODE OF PRACTICE; PATIENTS; INFECTION; TRANSPLANTATION...
Identifiers:

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